**Michael Kogan**
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# Curriculum Vitae



Born on November 17, 1971, German citizen, married have one daughter 16 years old.

**Professional target**
To be in a technical lead role at IC digital design and implementation team, work on challenging design on the edge of technology.

**Profile**
- Multicultural, Multilanguage, digital ASIC Design Engineer with more than 18 years experience (Taped out more than 30 designs).
- Have experience and technical skills allowed me to span the very wide range of Digital ASIC implementation flow (RTL to GDSII) in literally every single part of the flow.
- Have deep familiarity and hands on experience in physical implementation of Digital ICs in Automotive, Wireless Communications, Mobile Digital TV, Mobile Phones Hand held Devices, Health Care, Space applications, as well as System on Chip, High Speed, High Density and Low Power designs on the edge of technology process.
- Project planning, implementation, monitoring and quality validation.
- Customer ramp-up, methodology and design environment setup, know-how transfer.
- Self-motivated, working well as an individual or as part of a team, and able to work under high pressure.

# Professional experience

**Digital ASIC Implementation and DFT Consultant        Jan. 2014 – now**
 **Freelancer**
 Provide following services:
- Layout (physical implementation) of digital IC: RTL to GDSII
- Physical verification
- Timing and power analysis
- Design for test solutions: setup test concept, DFT insertion, test vector generation, low power ATPG, hierarchical test: core isolation, pattern retargeting, LBIST, scan compression: XOR, EDT
- RTL and Timing Constraint validation.
- Synthesis and Logic Equivalence Check.
- FPGA Design and Implementation
- Ramp up of young engineer, start-up teams.

**ASIC/FPGA  Engineer                              Feb .  2011 –Dec. 2013**
**Matis-Deutschland, Munich Germany**

Onsite and remote support of a customer from Automotive, Aerospace and Defence and Telecommunication market.
VHDL design,  Synthesis, Static timing analysis (STA),  DFT (scan insertion,  xor compression, stuck-at and at-speed ATPG),  Floorplan, CTS, timing closure, Place & Signal and power Route, IRDrop analysis and optimization of complex device at High Radiation(Space) technology, supervision of layout process implemented by subcontractor teams..
• EDA tools: Design Compiler, PrimeTime of Synopsys, Modelsim, Tessent of Mentor,  RTL Compiler, Encounter Test, EDI of Cadence  HiDFT-Signoff of Defacto

**Hardware  Designer                          Oct .  2009 – Jan. 2011**
 **Siemens Healthcare R&D department , Nuremberg Germany**

  • Design and implementation of Hardware Programmable Components for Medical devices such as Computer tomography.
 • VHDL coding from spec
 • RTL verification and optimization for Xilinx FPGA and CPLD technologies.
 • Formal Verification and RTL quality check.
 • Adaptation of an old code to new spec and technology requirement
 • Validation of FPGA and CPLD implementation in lab.
 • EDA tools: ISE of Xilinx, HDL-Designer of Modelsim, Conformal LEC of Cadence

**Freelancer DFT Consultant  at Micronas GmbH**, Munich Germany
                                        **Feb. 2009 – Sept 2009**

- Testability analysis of complex Digital TV design
- Stuck-at and at-Speed Automatic Test Pattern Generation (ATPG)
- Test coverage improves and test vector amount reduction
- EDA tools used: Encounter Test and Ncsim of Cadence.

**Lead Service Application Engineer**                    **May 2004 – Jan. 2009**
**Cadence Design Systems GmbH,** Munich, Germany
(IC Digital group of VCAD department)

- Project management: schedule and Statement of Work (SOW) definition and monitoring.
- Technical lead of flat (one man), and hierarchical (multi engineers) designs. Work in international teams (3-6 engineers) with colleagues from Russia, Israel, China, India and Europe.
- Physical implementation: RTL-synthesis trough Place and Route Layout implementation to Physical Verification and Tape-out to foundry of high-performance and ultra-low-power SOC devices at 180nm - 65nm technologies, for various customers from Russia, Israel and Europe.
- Design for Test (DFT)  expert
- Customer relationship:
  - Methodology and design environment setup
  - Ramp-up customer team to work with Cadence tools on IC digital design implementation, know-how transfer
- Trainings for both customer and internal teams on:
  RTL Compiler, SOC Encounter, Encounter Test, Conformal Logic Equivalence Check, with cooperation of Education Department of Cadence.
- EDA tools used: RTL Compiler, SOC Encounter, Celtic NDC, Fire and Ice (QX/QRC),  ETS, Power Meter, Voltage Storm, Encounter Test,  NCsim, Conformal Constraint Design, Conformal Logic Equivalence Check , PVS of Cadence.

**Study German language**                        **Oct. 2003 – Apr. 2004**
**Volkshochschule,** Munich, Germany

**Senior ASIC and FPGA Designer**                    **Nov. 2001 – Sept. 2003**
 **Avnet EMG GmbH,** Munich, Germany

- Technical lead.
- Layout of complex high speed (1 GHz) SOC designs with LVDS driver and receivers at LSI Logic 180nm technology, with Synopsys and LSI Logic tools, for a customer from Super Computer market in UK.
- DFT service: scan-chain and Jtag insertion, stuck-at ATPG and Iddq generation and simulation.
- FPGA design with Xilinx SpartanII technology
- EDA tools used: Design Compiler, DFT Compiler, Prime Time, VCS, Jupiter/Apollo of Synopsys, V-system of Mentor, FlexStream of LSI Logic,   Handle-C of Celoxica, Xilinx Project Navigator, Synplicity, FPGA Express of  Synopsys

**Senior ASIC Engineer**                        **Sep. 2000 – Oct. 2001**
**AST Ltd,** Ra'anana, Israel

- Technical lead.
- Distributor of NEC and Chip Express ASIC vendors in Israel.
- Front-end services: RTL validation and synthesis, scan-chain and Jtag insertion, stuck-at ATPG and Iddq generation and simulation, preparation for layout.

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- VHDL coding from spec. for Telecommunication and Medicine clients.
- ASIC to ASIC conversion from old to most recent ChipExpress technology
- Customer trainings, and flow setup.
- EDA tools used: Design Compiler, Primetime, VCS of Synopsys. Debussy of Novas, DFT tools of Syntest, Data Book (Escalade), Visual HDL (Innoveda), V-system of Mentor, OpenCAD of NEC, check_all of ChipExpress.

**ASIC Application Engineer**                                    **Oct. 1997 – Sep. 2000**
**AST Ltd**, Ra'anana, Israel
- Distributor of Chip Express ASIC vendors in Israel
- Front-end services: RTL validation and synthesis, scan-chain and Jtag insertion, stuck-at ATPG and Iddq generation and simulation, preparation for layout.
- FPGA to ASIC conversion from Xilinx and Altera to ChipExpress technology.
- EDA tools used: Leonardo of Exemplar, VCS of Viewlogic, DFT tools of Syntest, check_all of ChipExpress.

## Professional Trainings
- **Projekt Management –** keep it short and simple – TÜV SÜD Akademie
- **Quality in Projects** (Qualität in Projekten) – TÜV SÜD Akademie
- **Physical implementation** ( internal AE trainings at Cadence ) **:**
  SOC Encounter, Low Power Flow implementation with CPF
- **RTL coding and synthesis:**
  Encounter RTL Compiler of Cadence, Advanced Chip Synthesis using Design Compiler of Synopsys, Advanced VHDL
- **Design for Test** ( internal AE trainings at Cadence ) **:**
  RC-DFT, Encounter Test Jump Start and Deep Dive at Cadence
- **FPGA design:**
  Xilinx FPGA and tools for professionals, Handle C using DK1 of Celoxica
- **ASIC vendor tools for digital circuit implementation**:
  LSI FlexStream, NEC OpenCAD

## Education

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| 1995 – 1997 | • The state institute for technological training, College Tel-Hai, Israel. Electrical Engineering -. Electronics with the second direction Computer and Systems |
| 1989 – 1990 | • Technical school in Lvov, Ukraine<br>Electro-vacuum production |
| 1979 – 1989 | • School in Lvov, Ukraine |

- **Languages**: English, German, Russian, Hebrew are fluent, Ukrainian good
- **Customer's and colleague's feedback are available under**:
  http://www.linkedin.com/in/michaelkogan or http://www.ic-link.eu