REFERENCE PROJECTS OF MR. MICHAEL KOGAN DIGITAL IC LAYOUT AND DFT FREELANCER-CONSULTANT

INTRODUCTION

MR. MICHAEL KOGAN

- Career started in 1997, Freelancer since 2014
- Skill set span a unique wide range at all aspects of Digital ASIC Implementation (RTL to GDSII) flow, from RTL coding and synthesis through Design for Test and Place & Route implementation to Physical Verification and Tape-out to foundary

- Services:
  - Physical Implementation of Digital IC: Synthesis, STA, Place and Route
  - Design for test (DFT) solutions: scan insertion, hierarchical and low power DFT, test point insertion, cell aware, stuck-at & at-speed ATPG etc.
  - Spec to Packaged Chip: complete or partially outsourcing in cooperation with some design houses
  - Technology conversion: ASIC to ASIC, FPGA to FPGA, FPGA to ASIC etc…
  - Team or individual ramp-up
  - Methodology setup and optimization.
  - Onsite or remote support

CUSTOMERS

- Support international customers in EMEA and North America regions: Germany, France, Great Britain, Serbia, Israel, USA etc.

- Support customers from varios markets: Consumer electronic, Telecomunication, Automotive, Aerospace and Defence, Health Care, etc.

References can be provided on demand

PROJECT EXAMPLES

ADVANCED GPS/GALILEO ASIC

Description

The (Advanced GPS/GALILEO ASIC) is a radiation tolerant GNSS baseband ASIC capable of processing the modernized GPS and Galileo Signals. Due to its flexibility it is also able to process not only GPS and Galileo but also other GNSS systems like Glonass, Compass, etc.

Tasks

- RTL Synthesis to Hard Radiation Space dedicated Technology
- Static Timing Analysis (STA): Timing Constraints generation, multi scenario STA
- Scan Insertion
- Stuck-at and at-Speed Automatic Test Pattern Generation
- Preparation for Layout: Floor plan, Clock Tree Synthesis
- Interface and teamwork with Layout Team on Physical Implementation and Timing Closure.

Technical Environment

- Synopsis Design Compiler and Prime Time
- Mentor Tessent and Modelsim
- Defacto HIDFT-Signoff
- Cadence EDI

Client Reference :
EADS-Astrium , Germany

4G LTE – WIRELESS COMMUNICATION PROCESSOR

Description

4G LTE – wireless communication processor chip to provide fast and secure internet connection for modern mobile phone and other commercial devices.

Tasks

- Scan Chain XOR compression
- Stuck-at and at-Speed Automatic Test Pattern Generation
- Fault coverage improvement
- Reduction of test vectors amount
- Test vector simulation
- Static Timing Analysis

Technical Environment

- Cadence RTL Compiler, Encounter Test, Ncsim
- Synopsys: Prime Time

Client Reference :
Altair Semiconductor, Israel

HIGHLY PROGRAMMABLE DIGITAL PROCESSOR

Description

Special processor, for communication and data exchange between satellite on the orbit and ground based station. Pilot project at 65nm STM Space technology.

Tasks

- Static Timing Analysis (STA): Timing Constraints generation, multi scenario STA
- Scan Insertion
- Testability analysis and improvement atRTL
- Stuck-at and Delay-test Automatic Test Pattern Generation (ATPG)
- Support for layout team

Technical Environment

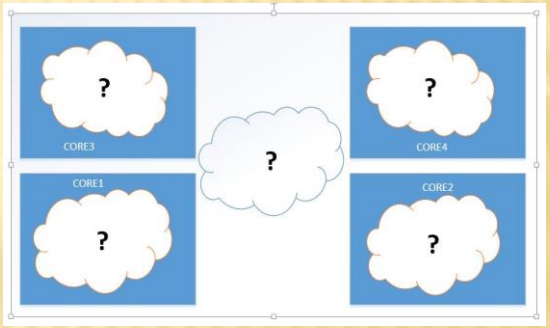
- Synopsis Design and DFT Compiler, Prime Time
- Mentor HDL-Designer, Tessent and Modelsim

Client Reference :

Airbus Defence & Space (Astrium), Germany

SETUP OF HIERARCHICAL TEST CONCEPT

- Hierarchical scan insertion
- Hierarchical scan chain compression macro (EDT) insertion
- Core Isolation (Core Wrapper Chains insertion, IEEE 1500)
- Hierarchical ATPG (INTEST, EXTEST)
- Pattern Retargeting
- Internal JTAG (iJTAG, IEEE 1687): test of embedded instruments, 3rd party IP



- Test point insertion
- Cell aware ATPG
- Stuck-at, at-Speed, IDDQ, pseudo random (LBIST) test pattern generation (ATPG)

Client Reference :
Infineon AG, Germany

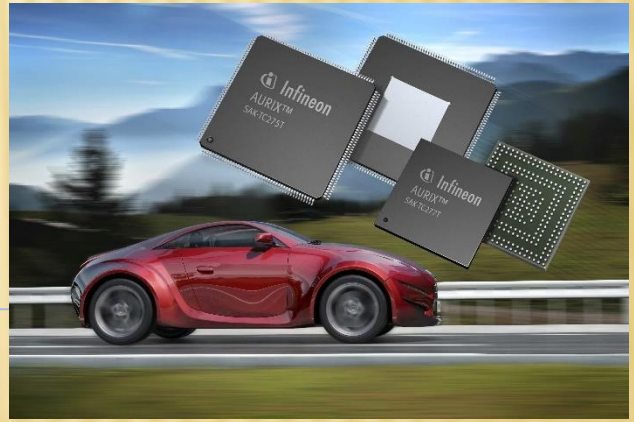
HIERARCHICAL SCAN INSERTION & ATPG OF MULTICORE MICROCONTROLLER FOR AUTOMOTIVE APPLICATION

Description

Evaluation of hierarchical test flow on subset of very complex multicore microcontroller for Automotive application, used 40nm and 28nm Infineon technologies.
DFT implementation of one complex partition with 300k registers and several dozen of Memories and IPs.

Tasks

- RTL Synthesis
- Scan Chains Insertion with integration of Mentor Compression (EDT) macro
- Mentor Test Points insertion to improve LBIST coverage
- Core isolation insertion with Wrapper Chains insertion
- Stuck-at and at-Speed Automatic Test Pattern Generation
- LBIST stuck at and at-speed Test Pattern Generation
- Test Patterns simulation with and without SDF



Technical Environment

- Synopsys Design and DFT Compiler
- Mentor Tessent
- Cadence Ncsim
- Infineon Camino design environment
- Clearcase version control tool

Client Reference :
Infineon AG, Germany

DFT IMPLEMENTATION OF SEVERAL PARTITIONS OF SATELITE COMMUNICATION SWITCH DEVICE, INTENDED FOR COMERCIAL SPACE APPLICATION

Description

DFT Implementation of 6 partitions of very complex design for Space application at 28nm ST Microelectronics
Technology (RelHi FDSOI 28), ~25Mio instances,
~3k Memories of different types.
Every partition include between 500k up to 1.1Mio registers, several dozen of RAMs and some analog IPs.

Tasks

- Scan Chain Insertion with Synopsys compression,
  On Chip Clock (OCC) insertion ,
  Core Wrapper Chains insertion,
  Integration of IEEE 1500 controller
- Stuck-at and at-Speed Automatic Test Pattern Generation
- Test points insertion to improve fault coverage

Technical Environment

- Synopsys Design and DFT Compiler, TetraMax (Tmax, TmaxII)
- STM FrontKit design environment
- SVN version control tool

Client Reference :
easiilc, France

HIERARCHICAL DFT IMPLEMENTATION OF COMPLEX IP FOR CONSUMER DEVICE

Description

System-On-Chip (SOC) for smart glasses cameras. Design contain over 10 Mio instances and over 200 Memories. Hierarchical physical and DFT implementation with Cadence EDA tools at 40nm TSMC low power technology

Tasks

- DFT Implementation of 1 partition with 2.5Mio instances
- Core and Wrapper Scan Chains insertion
- Insertion of Scan-Compressor and OCC modules
- Stuck-at and TFT ATPG
- Test patterns simulation
- Create timing constraints for all test modes, Static Timing Analysis (STA)

Technical Environment

- Synopsys Design and DFT Compiler, Prime Time, Tetra Max
- Cadence NCsim

Client Reference :
S3/Adesto, Ireland

RECOMMENDATIONS AND REFERENCES

REFERENCES

More recommendations can be found :

- LinkedIN profile: https://www.linkedin.com/in/michaelkogan
- http://www.ic-link.eu/references.html

Most recent training certificates:

- http://www.ic-link.eu/certificates.html

Online CV

- http://www.ic-link.eu/cv.html

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