REFERENCE PROJECTS OF MR. MICHAEL KOGAN DIGITAL IC LAYOUT AND DFT FREELANCER-CONSULTANT

INTRODUCTION

MR. MICHAEL KOGAN

- Career started in 1997, Freelancer since 2014
- Skill set span a unique wide range at all aspects of Digital ASIC Implementation (RTL to GDSII) flow, from RTL coding and synthesis through Design for Test and Place & Route implementation to Physical Verification and Tape-out to foundary

- Services:
  - Physical Implementation of Digital IC: Synthesis, STA, Place and Route
  - Design for test (DFT) solutions: scan insertion, hierarchical and low power DFT, test point insertion, cell aware, stuck-at & at-speed ATPG etc.
  - Spec to Packaged Chip: complete or partially outsourcing in cooperation with some design houses
  - Technology convertion: ASIC to ASIC, FPGA to FPGA, FPGA to ASIC etc…
  - Team or individual ramp-up
  - Methodology setup and optimization.
  - Onsite or remote support

CUSTOMERS

- Support international customers in EMEA and North America regions: Germany, Great Britain, Serbia, Israel, USA etc.

- Support customer from varios markets: Consumer electronic, Telecomunication, Automotive, Aerospace and Defence, Health Care, etc.

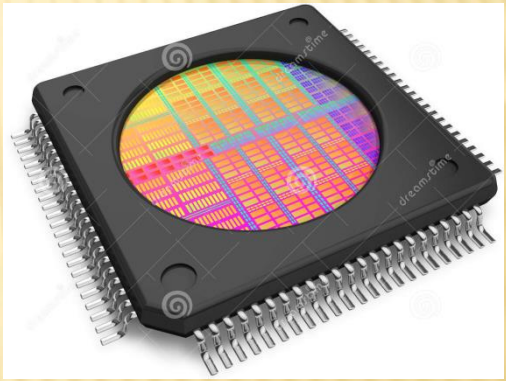
References can be provided on demand

PROJECT EXAMPLES

LAYOUT OF NETWORK PROZESSOR

Description

Network Processor , 120 Mio. Instances, over 1.000 RAMS, average system frequency over 500 MHz, Flip Chip package, 6 RC corners , 4 library sets, multiple functional and test Timing Modes, 28nm TSMC technology. USA based customer.



Tasks

- Physical Implementation (Floorplan, Placement, Clock and Signal Routing, Xtalk analysis and repair) of 3 sub-blocks, up to 3.5 Million instances each
- Timing closure
- Static Timing Analysis (STA)
- Power consumption at IRdrop reduction
- Physical Verification

Technical Environment

- Cadence EDI, Tempus, Voltus, PVS, Conformal-LEC

Client Reference :

Cadence Design Systems, Germany

LAYOUT OF NETWORK CAMERA AND VIDEO SERVER PLATFORM DESIGN

Description

System-On-Chip (SOC) for networked surveillance cameras Over 25Mio. gates, almost 450 Memories with total 30Mbit , hierarchical physical implementation with Cadence EDA tools at 28nm TSMC energy-efficient and high-performance technology

Tasks

- Physical Implementation of 3 sub-blocks, up to 3.5 Million instances each
- Timing closure
- Static Timing Analysis (STA)
- Power consumption at IRdrop reduction
- Physical Verification

Technical Environment

- Cadence EDI, Tempus, Voltus, PVS, Conformal-LEC, custom flow management tools

Client Reference :

Renesas Electronic Europe, Germany

IMPELENTATION OF HIGHLY PROGRAMMABLE DIGITAL PROCESSOR

Description

Special processor, for communication and data exchange between satellite on the orbit and ground based station. Pilot project at 65nm STM Space technology.

Tasks

- Static Timing Analysis (STA): Timing Constraints generation, multi scenario STA
- Scan Insertion
- Testability analysis and improvement atRTL
- Stuck-at and Delay-test Automatic Test Pattern Generation (ATPG)
- Support for layout team

Technical Environment

- Synopsis Design and DFT Compiler, Prime Time
- Mentor HDL-Designer, Tessent and Modelsim

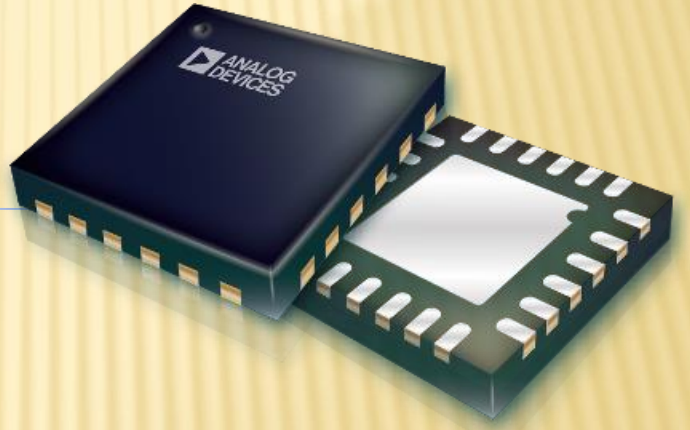
Client Reference :

Airbus Defence & Space (Astrium), Germany

IMPLEMENTATION OF SMALL DIGITAL CORES INSIDE OF ANALOG DESIGN

Description

DFT Implementation of 2 digital partitions inside of complex analog design at 40nm



Tasks

- Synthesis
- Floorplan
- Place and Route
- Timing Closure
- Static Timing
- Power Consumption and Rail Analysis

Technical Environment

- Genus , Innovus, Tempus, Voltus of Cadence

Client Reference :
Analog Devices, Ireland

PHYSICAL IMPLEMENTATION OF COMPLEX IP FOR CONSUMER DEVICE

Description

System-On-Chip (SOC) for smart glasses cameras. Design contain over 10 Mio instances and over 200 Memories. Hierarchical physical and DFT implementation with Cadence EDA tools at 40nm TSMC low power technology

Tasks

- Physical Implementation of 1 partition with 2.5Mio instances
- Synthesis & Scan insertion
- Florplan & Timing closure
- Static Timing Analysis (STA)
- Power consumption at IRdrop reduction

Technical Environment

- Synopsys Design and DFT Compiler, Prime Time, Tetra Max
- Cadence Innovuse, Conformal-LEC, custom flow management tools

Client Reference :
S3/Adesto, Ireland

RECOMMENDATIONS AND REFERENCES

REFERENCES

More recommendations can be found :

- https://www.linkedin.com/in/michaelkogan
- http://www.ic-link.eu/references.html

Most recent training certificates:

- http://www.ic-link.eu/certificates.html

Online CV

- http://www.ic-link.eu/cv.html

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